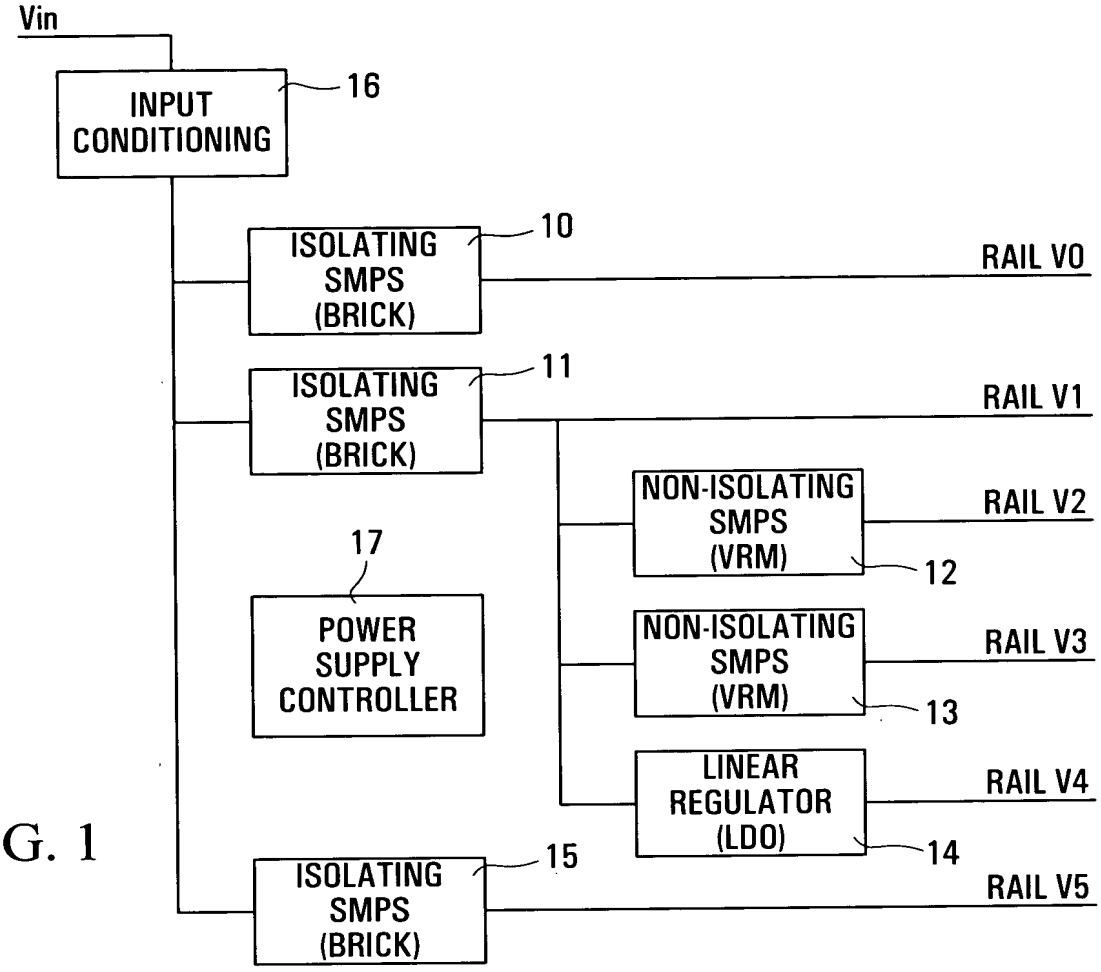

Vin
INPUT CONDITIONING
16
ISOLATING SMPS (BRICK)
10
RAIL V0
ISOLATING SMPS (BRICK)
11
RAIL V1
NON-ISOLATING SMPS (VRM)
RAIL V2
12
17
POWER SUPPLY CONTROLLER
NON-ISOLATING SMPS (VRM)
RAIL V3
13
LINEAR REGULATOR (LDO)
RAIL V4
14
ISOLATING SMPS (BRICK)
15
RAIL V5

FIG. 1

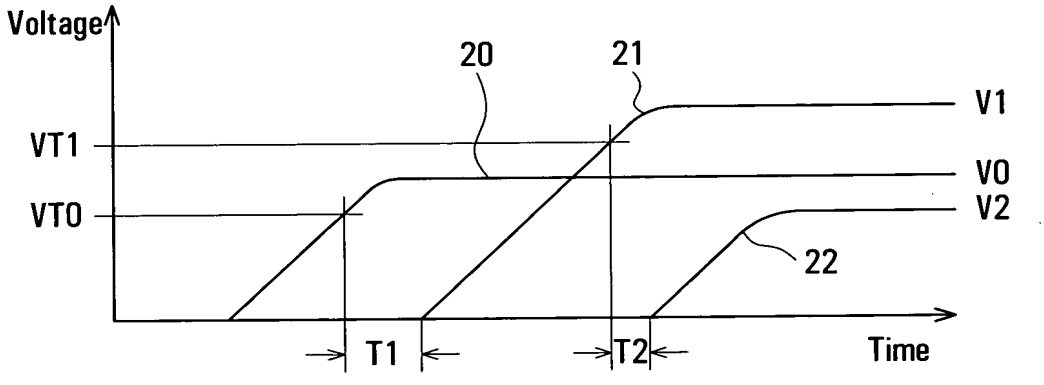

Voltage
20
21
V1
VT1
V0
VT0
V2
22
T1
T2
Time

FIG. 2

FIG. 3

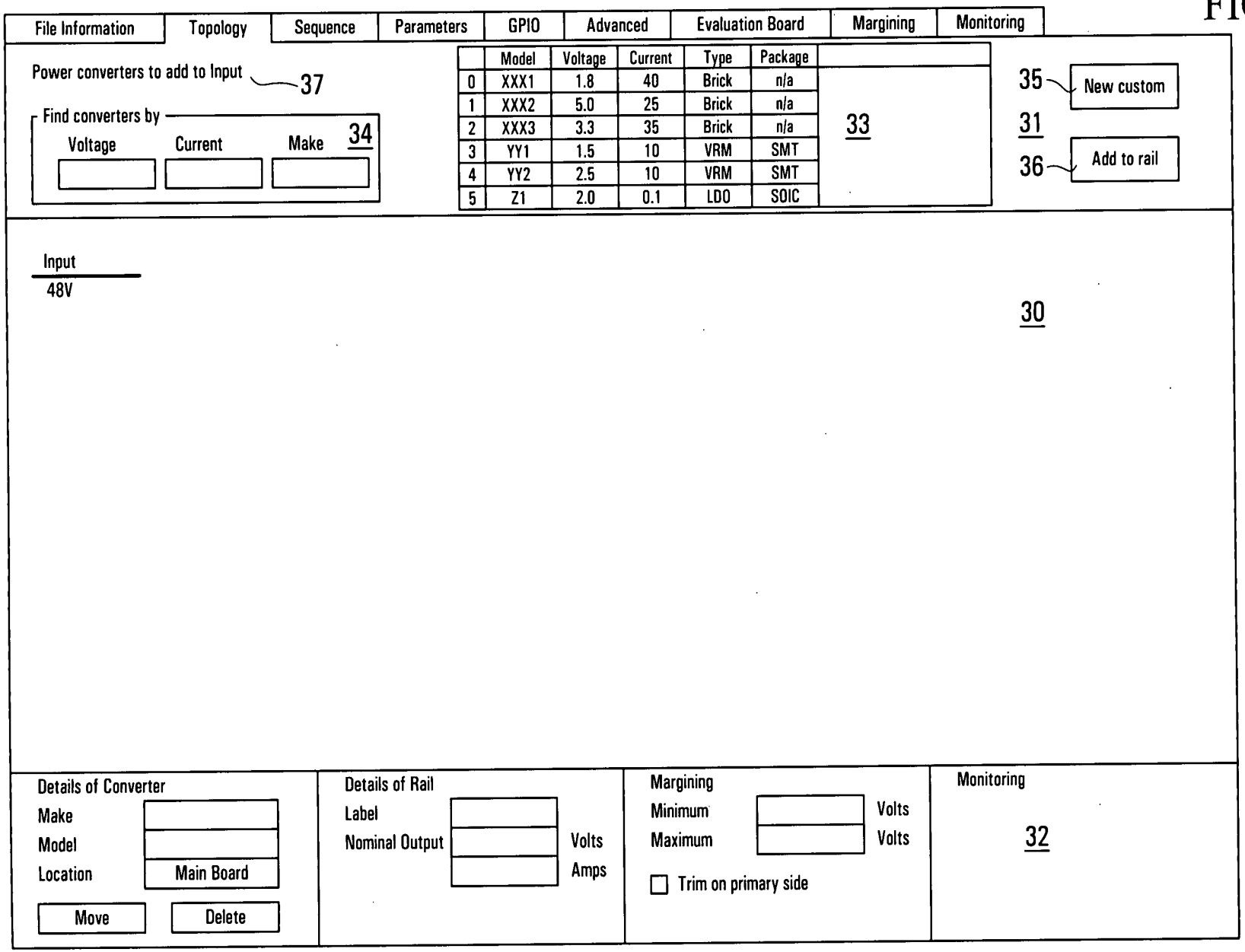

File Information
Topology
Sequence
Parameters
GPIO
Advanced
Evaluation Board
Margining
Monitoring
Power converters to add to Input
37
Find converters by
Voltage
Current
Make
34
Model
Voltage
Current
Type
Package
0 XXX1 1.8 40 Brick n/a
1 XXX2 5.0 25 Brick n/a
2 XXX3 3.3 35 Brick n/a
3 YY1 1.5 10 VRM SMT
4 YY2 2.5 10 VRM SMT
5 Z1 2.0 0.1 LDO SOIC
33
35
New custom
31
36
Add to rail
Input
48V
30
Details of Converter
Make
Model
Location
Main Board
Move
Delete
Details of Rail
Label
Nominal Output
Volts
Amps
Margining
Minimum
Maximum
Volts
Volts
Trim on primary side
Monitoring
32

FIG. 4

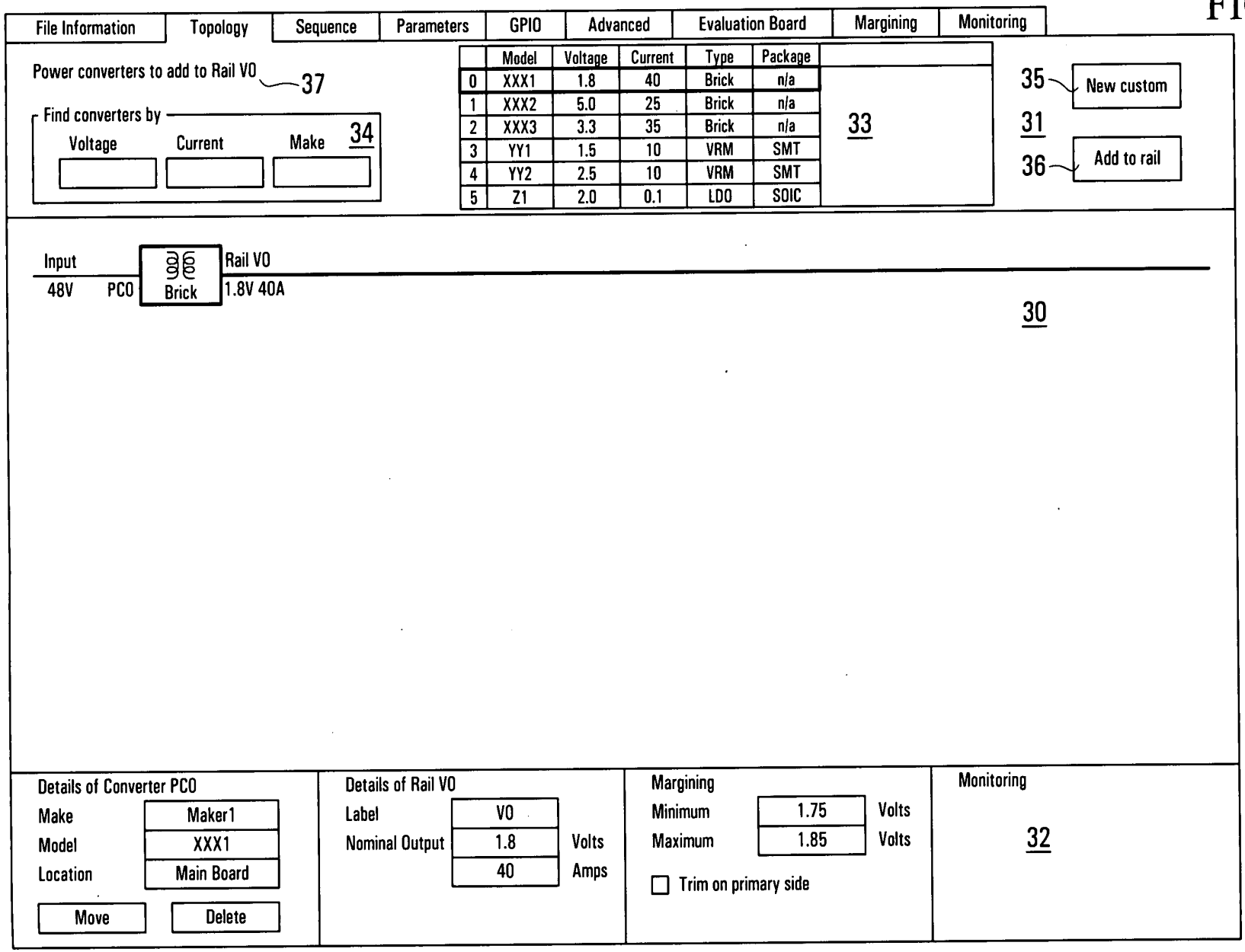

File Information
Topology
Sequence
Parameters
GPIO
Advanced
Evaluation Board
Margining
Monitoring
Power converters to add to Rail V0
37
Find converters by
Voltage
Current
Make
34
Model
Voltage
Current
Type
Package
0 XXX1 1.8 40 Brick n/a
1 XXX2 5.0 25 Brick n/a
2 XXX3 3.3 35 Brick n/a
3 YY1 1.5 10 VRM SMT
4 YY2 2.5 10 VRM SMT
5 Z1 2.0 0.1 LDO SOIC
33
35
New custom
31
36
Add to rail
Input
48V
PC0
Brick
Rail V0
1.8V 40A
30
Details of Converter PC0
Make
Maker1
Model
XXX1
Location
Main Board
Move
Delete
Details of Rail V0
Label
V0
Nominal Output
1.8
Volts
40
Amps
Margining
Minimum
1.75
Volts
Maximum
1.85
Volts
Trim on primary side
Monitoring
32

FIG. 5

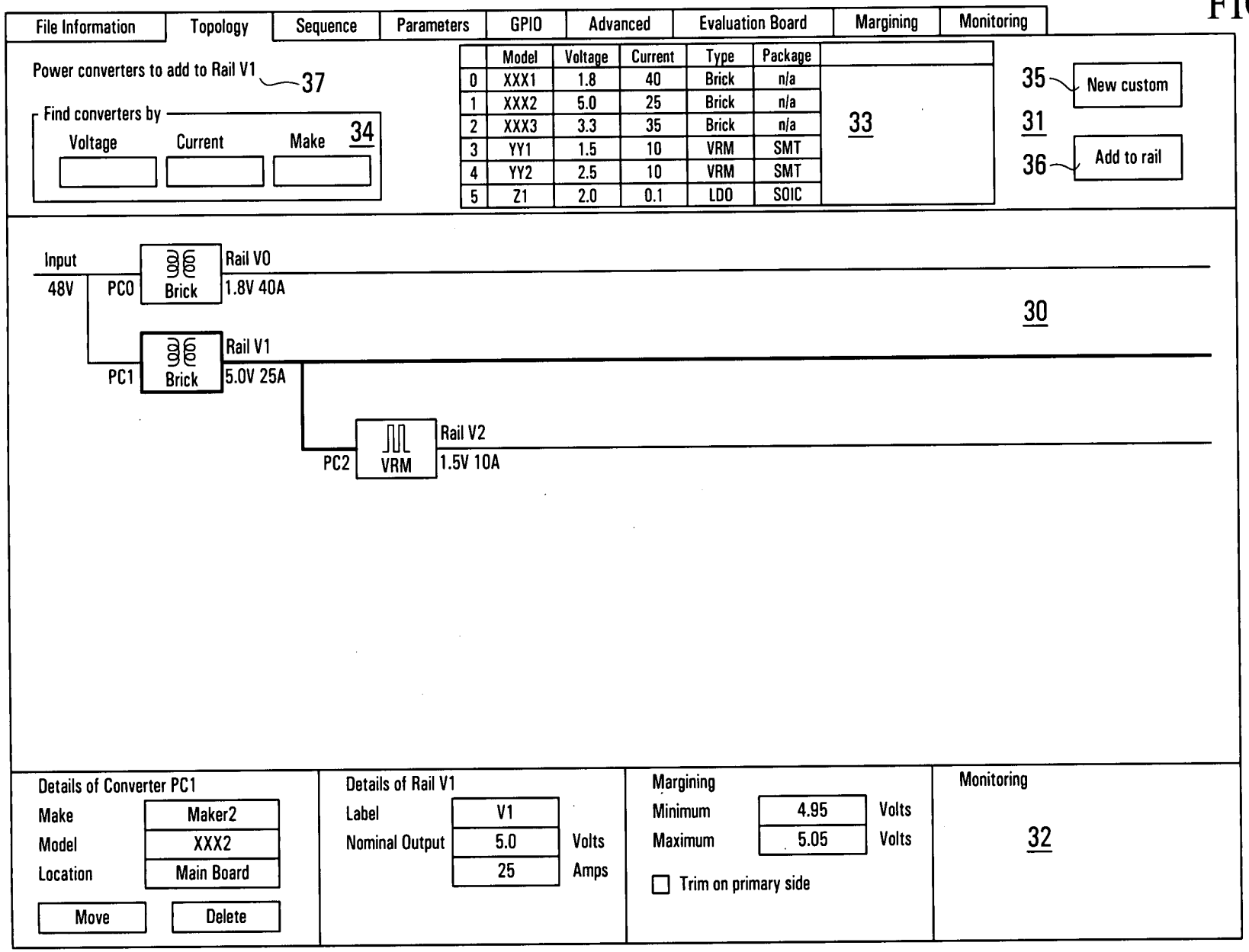

File Information
Topology
Sequence
Parameters
GPIO
Advanced
Evaluation Board
Margining
Monitoring
Power converters to add to Rail V1
37
Find converters by
Voltage
Current
Make
34
Model Voltage Current Type Package
0 XXX1 1.8 40 Brick n/a
1 XXX2 5.0 25 Brick n/a
2 XXX3 3.3 35 Brick n/a
3 YY1 1.5 10 VRM SMT
4 YY2 2.5 10 VRM SMT
5 Z1 2.0 0.1 LDO SOIC
33
35
New custom
31
36
Add to rail
Input
48V
PC0
Brick
Rail V0
1.8V 40A
30
PC1
Brick
Rail V1
5.0V 25A
PC2
VRM
Rail V2
1.5V 10A
Details of Converter PC1
Make
Maker2
Model
XXX2
Location
Main Board
Move
Delete
Details of Rail V1
Label
V1
Nominal Output
5.0
Volts
25
Amps
Margining
Minimum
4.95
Volts
Maximum
5.05
Volts
Trim on primary side
Monitoring
32

FIG. 6

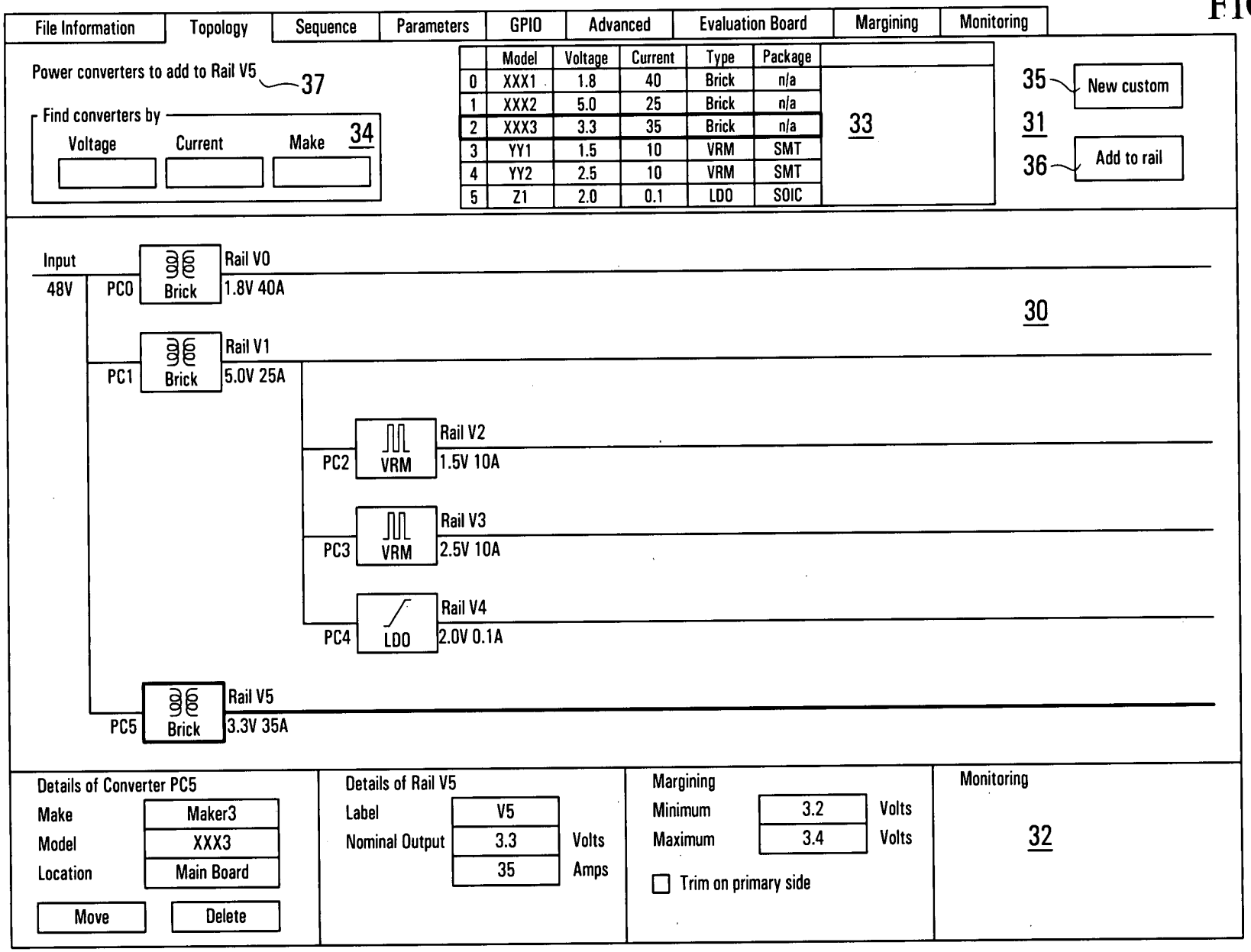

File Information
Topology
Sequence
Parameters
GPIO
Advanced
Evaluation Board
Margining
Monitoring
Power converters to add to Rail V5
37
Find converters by
Voltage
Current
Make
34
Model Voltage Current Type Package
0 XXX1 1.8 40 Brick n/a
1 XXX2 5.0 25 Brick n/a
2 XXX3 3.3 35 Brick n/a
3 YY1 1.5 10 VRM SMT
4 YY2 2.5 10 VRM SMT
5 Z1 2.0 0.1 LDO SOIC
33
35
New custom
31
36
Add to rail
Input
48V
PC0
Brick
Rail V0
1.8V 40A
30
PC1
Brick
Rail V1
5.0V 25A
PC2
VRM
Rail V2
1.5V 10A
PC3
VRM
Rail V3
2.5V 10A
PC4
LDO
Rail V4
2.0V 0.1A
PC5
Brick
Rail V5
3.3V 35A
Details of Converter PC5
Make
Maker3
Model
XXX3
Location
Main Board
Move
Delete
Details of Rail V5
Label
V5
Nominal Output
3.3
Volts
35
Amps
Margining
Minimum
3.2
Volts
Maximum
3.4
Volts
Trim on primary side
Monitoring
32

FIG. 7

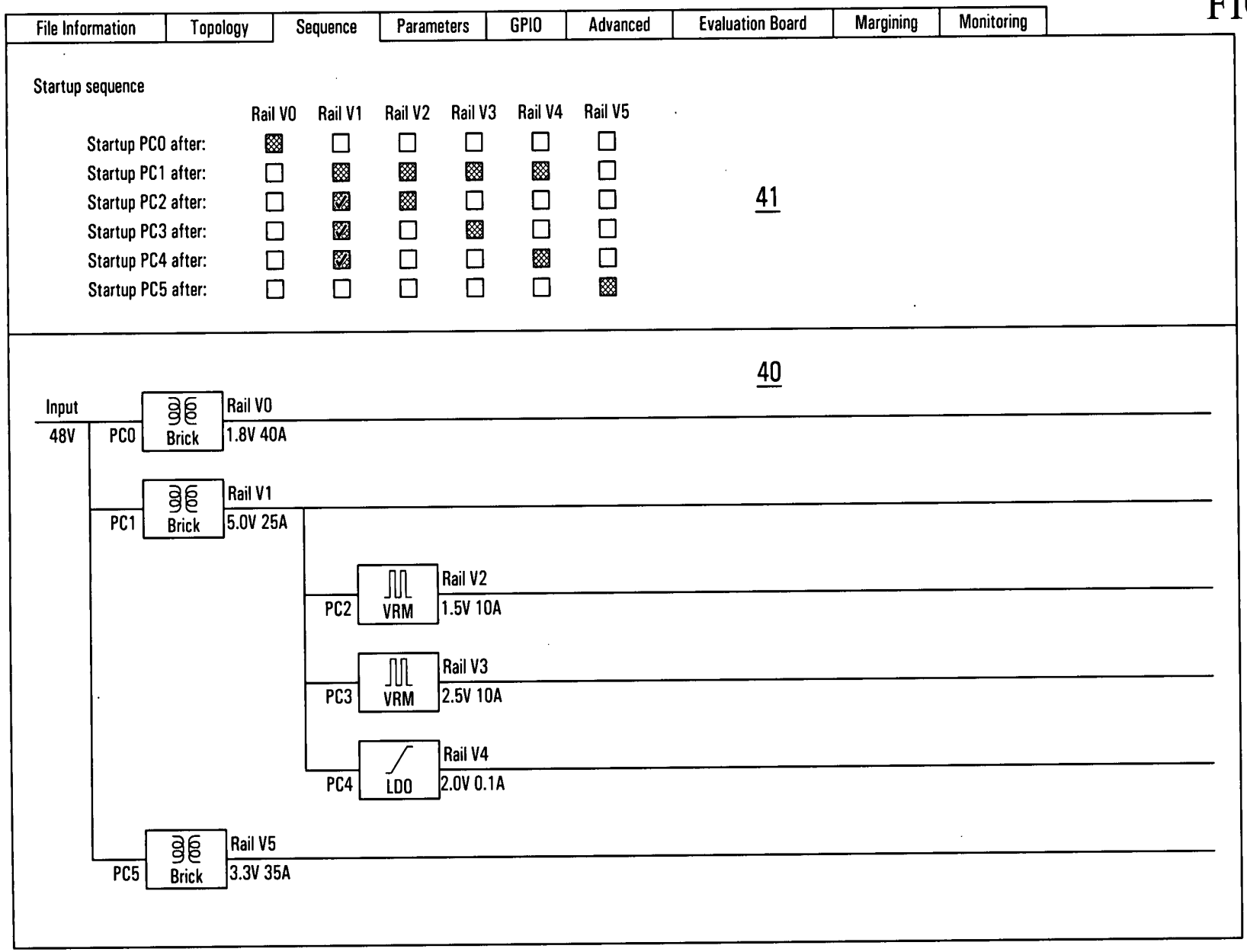

File Information
Topology
Sequence
Parameters
GPIO
Advanced
Evaluation Board
Margining
Monitoring
Startup sequence
Rail V0
Rail V1
Rail V2
Rail V3
Rail V4
Rail V5
Startup PC0 after:
Startup PC1 after:
Startup PC2 after:
Startup PC3 after:
Startup PC4 after:
Startup PC5 after:
41
40
Input
48V
PC0
Brick
Rail V0
1.8V 40A
PC1
Brick
Rail V1
5.0V 25A
PC2
VRM
Rail V2
1.5V 10A
PC3
VRM
Rail V3
2.5V 10A
PC4
LDO
Rail V4
2.0V 0.1A
PC5
Brick
Rail V5
3.3V 35A

FIG. 8

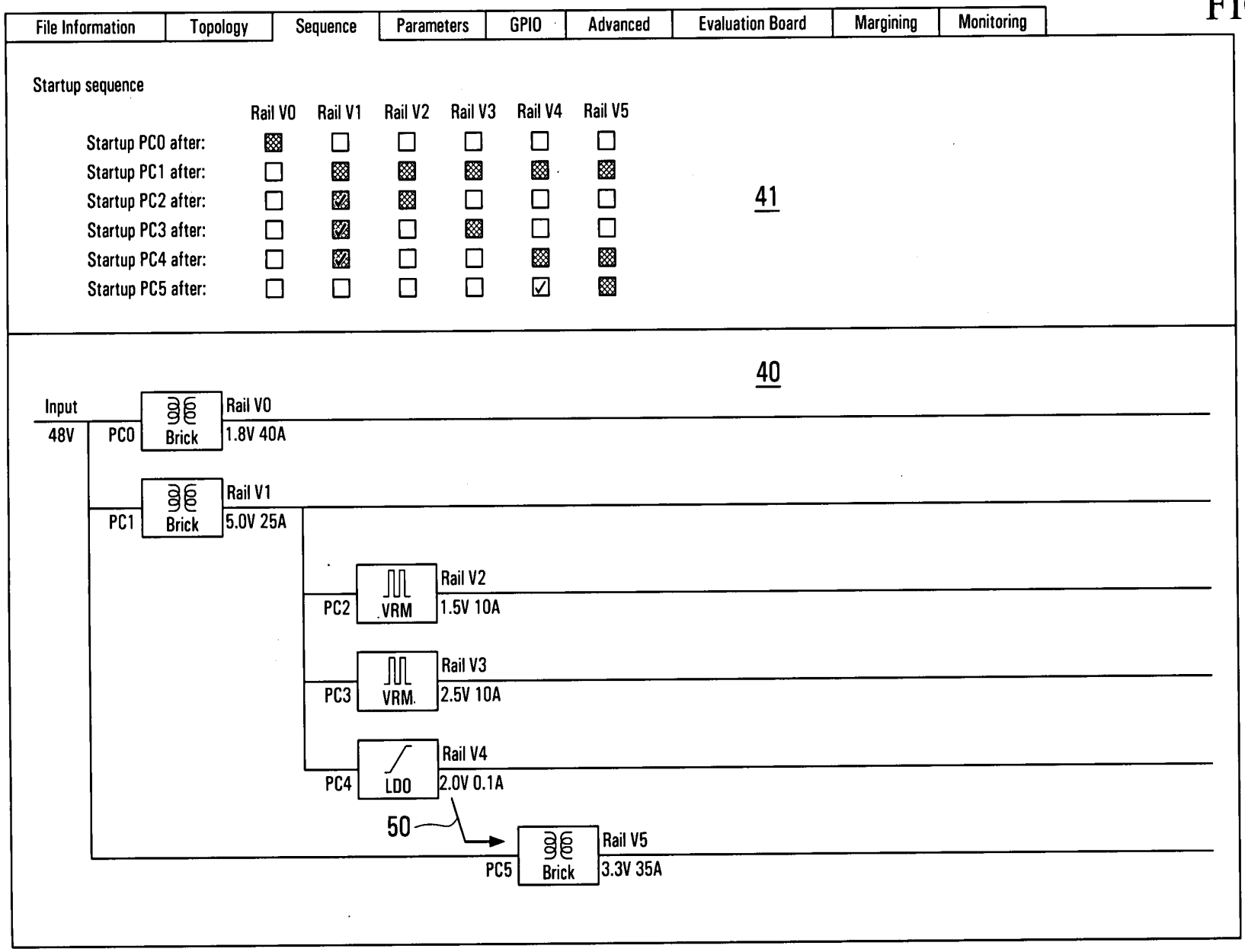

File Information
Topology
Sequence
Parameters
GPIO
Advanced
Evaluation Board
Margining
Monitoring
Startup sequence
Rail V0
Rail V1
Rail V2
Rail V3
Rail V4
Rail V5
Startup PC0 after:
Startup PC1 after:
Startup PC2 after:
Startup PC3 after:
Startup PC4 after:
Startup PC5 after:
41
40
Input
48V
PC0
Brick
Rail V0
1.8V 40A
PC1
Brick
Rail V1
5.0V 25A
PC2
VRM
Rail V2
1.5V 10A
PC3
VRM
Rail V3
2.5V 10A
PC4
LDO
Rail V4
2.0V 0.1A
50
PC5
Brick
Rail V5
3.3V 35A

FIG. 9

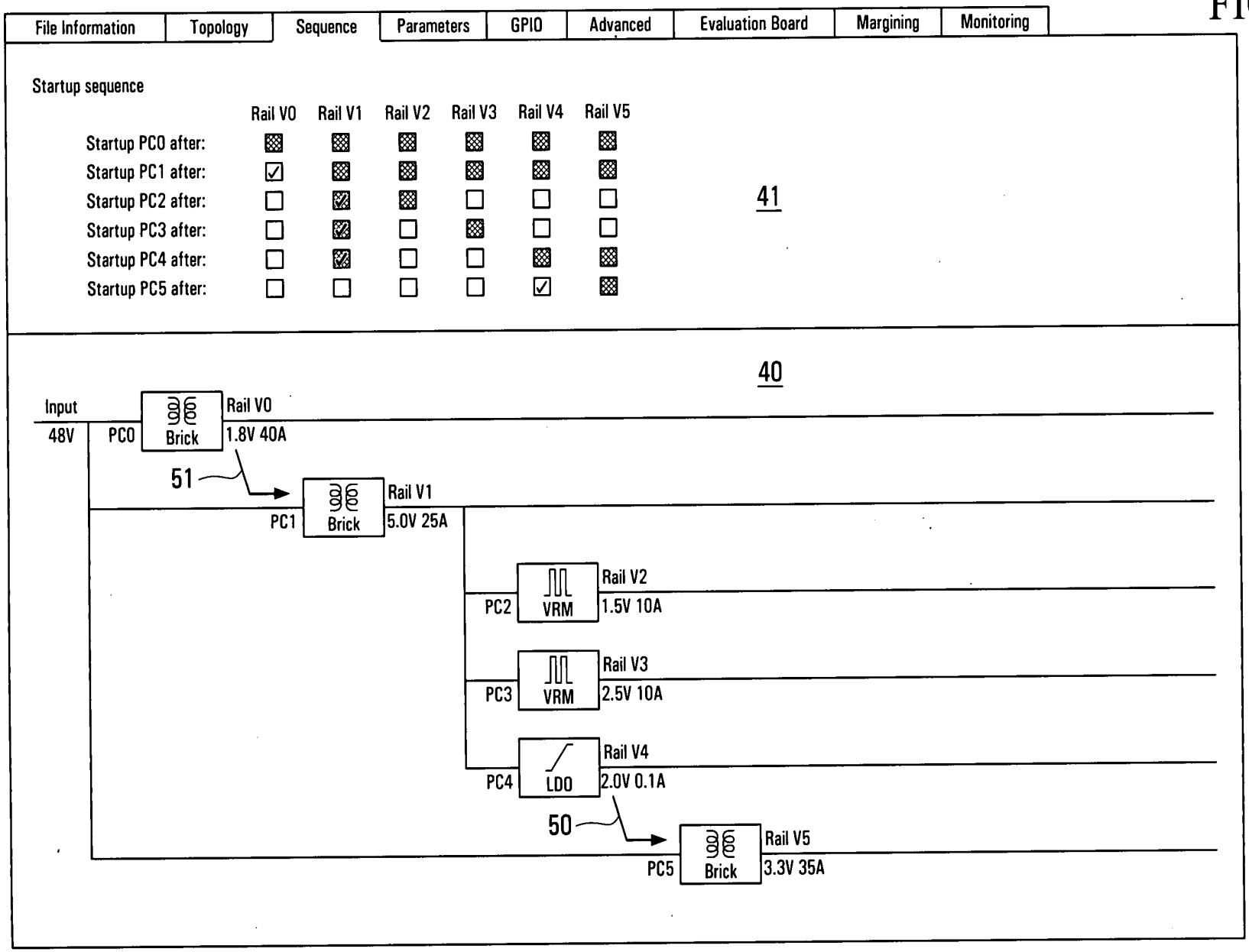

File Information
Topology
Sequence
Parameters
GPIO
Advanced
Evaluation Board
Margining
Monitoring
Startup sequence
Rail V0
Rail V1
Rail V2
Rail V3
Rail V4
Rail V5
Startup PC0 after:
Startup PC1 after:
Startup PC2 after:
Startup PC3 after:
Startup PC4 after:
Startup PC5 after:
41
40
Input
48V
PC0
Brick
Rail V0
1.8V 40A
51
PC1
Brick
Rail V1
5.0V 25A
PC2
VRM
Rail V2
1.5V 10A
PC3
VRM
Rail V3
2.5V 10A
PC4
LDO
Rail V4
2.0V 0.1A
50
PC5
Brick
Rail V5
3.3V 35A

FIG. 10

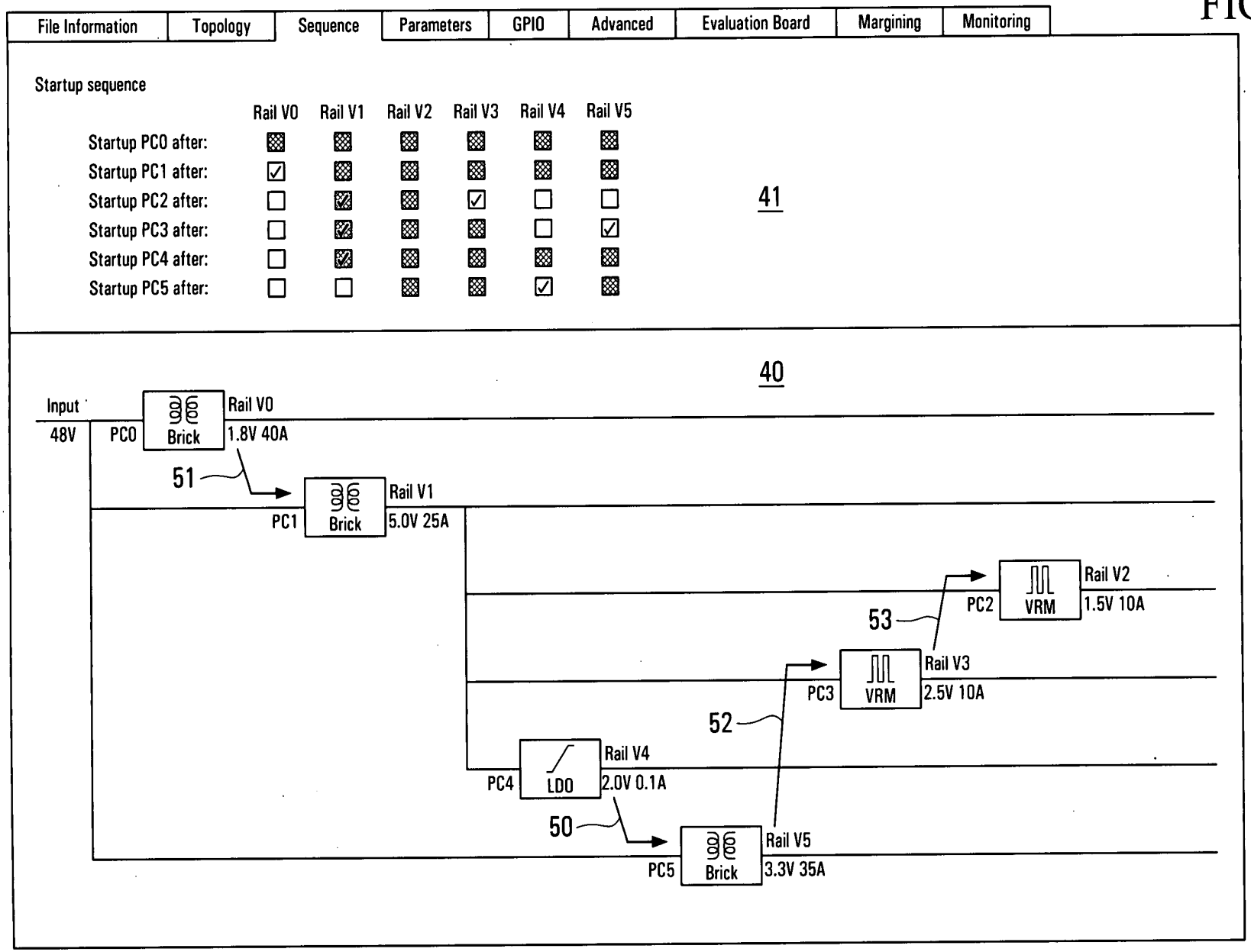
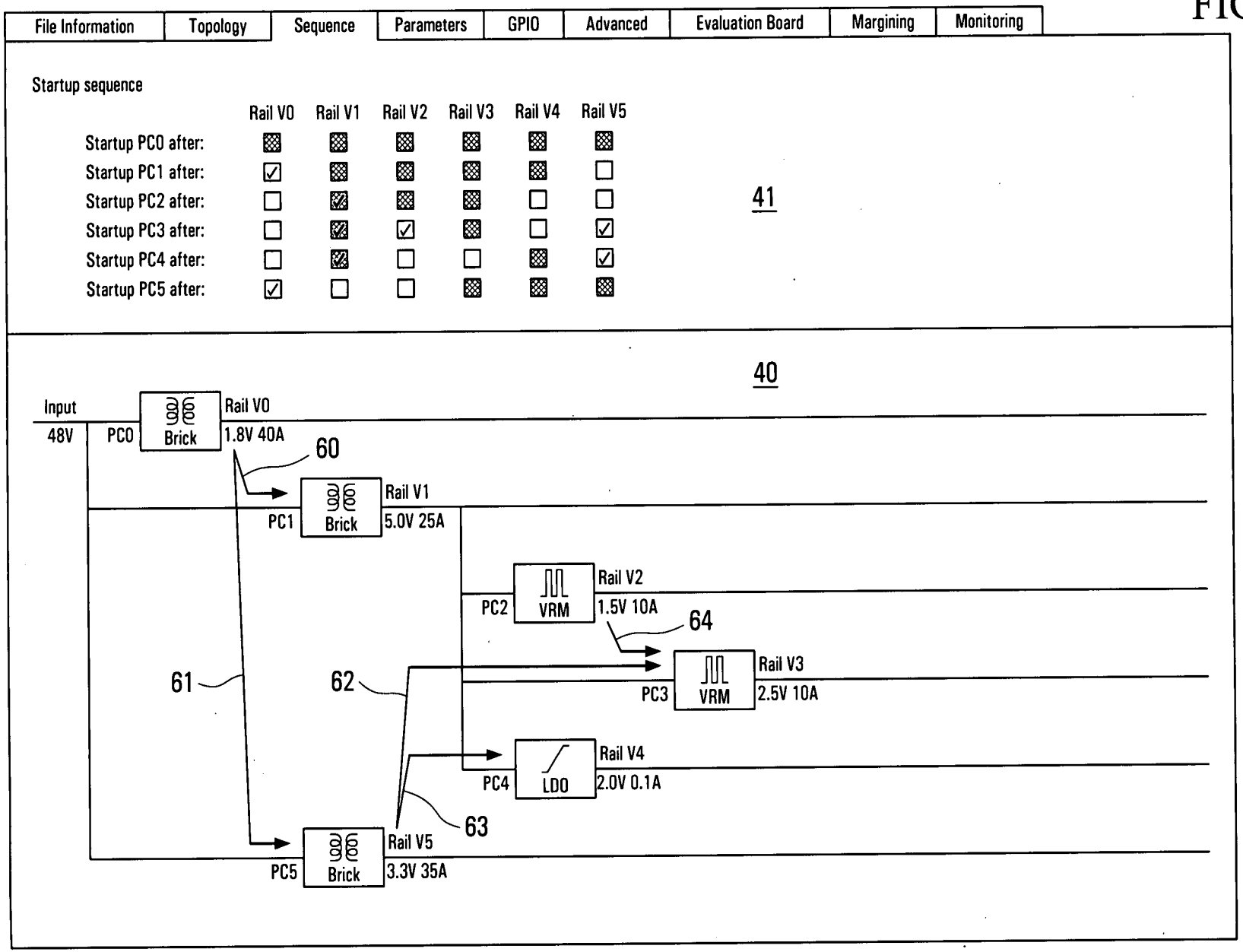

File Information
Topology
Sequence
Parameters
GPIO
Advanced
Evaluation Board
Margining
Monitoring
Startup sequence
Rail V0
Rail V1
Rail V2
Rail V3
Rail V4
Rail V5
Startup PC0 after:
Startup PC1 after:
Startup PC2 after:
Startup PC3 after:
Startup PC4 after:
Startup PC5 after:
41
40
Input
48V
PC0
Brick
Rail V0
1.8V 40A
51
PC1
Brick
Rail V1
5.0V 25A
53
PC2
VRM
Rail V2
1.5V 10A
PC3
VRM
Rail V3
2.5V 10A
52
PC4
LDO
Rail V4
2.0V 0.1A
50
PC5
Brick
Rail V5
3.3V 35A

FIG. 11


File Information
Topology
Sequence
Parameters
GPIO
Advanced
Evaluation Board
Margining
Monitoring
Startup sequence
Rail V0
Rail V1
Rail V2
Rail V3
Rail V4
Rail V5
Startup PC0 after:
Startup PC1 after:
Startup PC2 after:
Startup PC3 after:
Startup PC4 after:
Startup PC5 after:
41
40
Input
48V
PC0
Brick
Rail V0
1.8V 40A
60
PC1
Brick
Rail V1
5.0V 25A
PC2
VRM
Rail V2
1.5V 10A
64
61
62
PC3
VRM
Rail V3
2.5V 10A
PC4
LDO
Rail V4
2.0V 0.1A
63
PC5
Brick
Rail V5
3.3V 35A

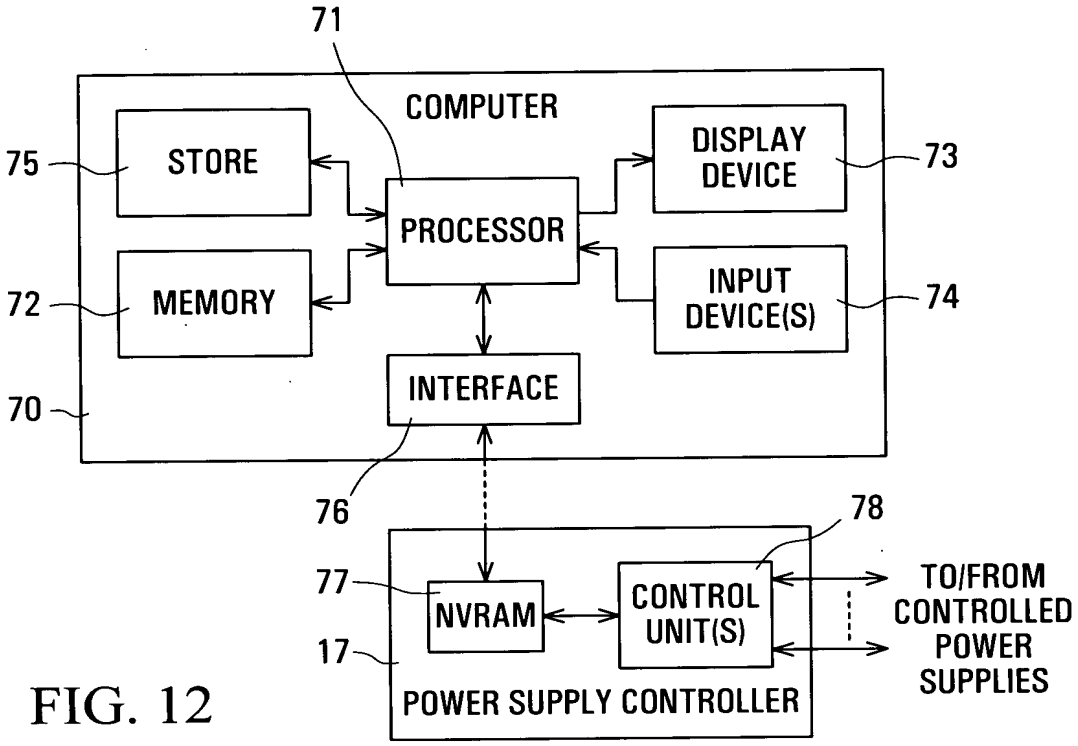

71
COMPUTER
75
STORE
PROCESSOR
DISPLAY DEVICE
73
72
MEMORY
INPUT DEVICE(S)
74
INTERFACE
70
76
78
77
NVRAM
CONTROL UNIT(S)
TO/FROM CONTROLLED POWER SUPPLIES
17
POWER SUPPLY CONTROLLER

FIG. 12


BIT: 7 6 5 4 3 2 1 0
CONFIG 0 0 1 1 1 1 1 1
STRTEN(0) 0 1 0 0 0 0 0 0
SHDNEN(0) 0 0 0 0 0 0 1 0
STRTEN(1) 0 0 0 0 0 0 0 1
SHDNEN(1) 0 0 0 1 0 0 0 0
STRTEN(2) 0 0 0 0 1 0 0 0
SHDNEN(2) 0 1 0 0 0 0 0 0
STRTEN(3) 0 0 1 0 0 0 0 0
SHDNEN(3) 0 0 0 0 0 1 0 0
STRTEN(4) 0 0 0 0 0 0 1 0
SHDNEN(4) 0 0 1 0 0 0 0 0
STRTEN(5) 0 0 0 1 0 0 0 0
SHDNEN(5) 0 0 0 0 1 0 0 0

FIG. 13